

Amendment under 37 CFR § 1.111

Serial No. 10/780,701

Attorney Docket No. 042113

**AMENDMENTS TO THE DRAWINGS**

The attached replacement sheets of drawings include changes to Figs. 1-4.

Amendment under 37 CFR § 1.111  
Serial No. 10/780,701  
Attorney Docket No. 042113

**REMARKS**

**Drawings**

Drawings have been objected to. The Examiner alleged that Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated.

Figures 1-4 have been designated by a legend --Related Art-- which is consistent with the description in the specification, such as "BRIEF DESCRIPTION OF THE DRAWINGS."

**Objection**

**Claim 20 was objected to because of the informalities.**

Accordingly, claim 20 has been amended to overcome the objection.

**Rejections under 35 USC §102(e)**

**Claims 1, 2, 4, 5, 7, 9 and 13-16 were rejected under 35 USC §102(e) as being anticipated by Matsunaga (U.S. Patent No. 6,670,710).**

Claim 1 has been amended to recite "said first multilayer interconnection structure including a pillar extending from a surface of said substrate and reaching at least said second multilayer interconnection structure, said pillar being formed in a region of said substrate right underneath said electrode pad."

Matsunaga describes that "As shown in FIG. 1, a via ring 30 is formed along the periphery of a chip 10. The via ring 30 surrounds the device area of the chip 10." (Col. 4, line

Amendment under 37 CFR § 1.111  
Serial No. 10/780,701  
Attorney Docket No. 042113

13-16). Thus, reference numeral 30 which appears like a pillar in Figs. 2-11 is a via ring.

Matsunaga explains about the via ring as follows:

As shown in FIGS. 12 and 13, . . . . A via ring 81, which is made by the first and second wiring layers 74 and 77, the contact plug 75 and the via 78, is formed along the periphery of a chip 70. **The via ring 81 is intended to prevent cracks at the time of scribing.**

In the structure of the first example of the prior art, the passivation film 84 is not a single-layer film. It is a laminated film made up of the PSG film 79 (or another type of SiO<sub>2</sub> film) and the SiN film 80 formed on the PSG film 79. This laminated structure serves to suppress the total stress of the film. The structure of the first example of the prior art raises a problem if an opening is formed in the passivation film 84 to provide a pad window. If such an opening is formed, the PSG film 79 is exposed in the wall surface of the opening. Since the exposed portion of the PSG film 79 undesirably serves as an inlet of moisture, it is hard to prevent the water or moisture from entering the chip.

In the process of forming the contact plug 75 and the wiring layers 74 and 77 by use of an Al material, **the via ring 81 serves to prevent water from entering the chip from the side portions of the chip.** This advantage cannot be expected if the contact plug 75 is formed of W.

(Col. 2, line 32 to 67). The via ring is formed to prevent cracks at the time of scribing and the via ring 81 serves to prevent water from entering the chip from the side portions of the chip.

In Matsunaga, passivation film is formed over the via ring and the via ring is not “formed in a region of said substrate right underneath said electrode pad.”

For at least these reasons, claim 1 patentably distinguishes over Matsunaga. Claims 2, 4, 5, 7, 9 and 13-16, depending from claim 1 also patentably distinguish over Matsunaga for at least the same reasons.

Amendment under 37 CFR § 1.111  
Serial No. 10/780,701  
Attorney Docket No. 042113

**Rejections under 35 USC §103(a)**

**Claim 8 was rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710) as applied to claim 1 above, and further in view of Nakajima et al. (U.S. Patent Publication No. 2003/0230809 A1).**

Claim 8 depends from claim 1, thus claim 8 patentably distinguishes over Matsunaga for at least the same reasons.

Nakajima et al is cited for allegedly disclosing that the pillars (16D, 24D, 26D, and 34D) provide mechanical support and reinforcement to the electrode pad (36) during a wire bonding process. Nakajima et al describes about the dummy plug as follows:

[0032] The dummy plugs and dummy wiring layers containing a refractory metal excel in tenacity over the interlayer insulating film. With a plurality of stacked structures each comprised of a dummy plug and a dummy wiring layer in contact thereto, **even if a crack occurs while a wire is being ultrasonically bonded to a pad, the crack is stopped by the dummy plug or dummy wiring layer, and therefore prevented from running over.**

However, crack during wire bonding has nothing to do with the via ring disclosed in Matsumura. Therefore, there is no suggestion or motivation for a person of ordinary skill in the art to apply the teaching of Nakajima et al to the via ring of Matsunaga. Moreover, even a person of ordinary skill in the art tried to combine the teachings of Matsunaga and Nakajima et al, it would not be obvious how these teachings can be combined.

Amendment under 37 CFR § 1.111

Serial No. 10/780,701

Attorney Docket No. 042113

Furthermore, as the Examiner admits, neither Matsunaga nor Nakajima et al discloses that a “pillar is formed in plural numbers so as to occupy at least 15% of the area of said region of said substrate right underneath said electrode pad as a whole” as recited in claim 8.

For at least these reasons, claim 8 patentably distinguishes over Matsunaga and Nakajima et al.

**Claims 10-12 and 17-19 were rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710) as applied to claim 1 above, and further in view of the Applicant’s Prior Art Figures 1-4 (APAF).**

Claims 10-12 and 17-19 all directly or indirectly depend from claim 1.

APAF has been cited allegedly disclosing on the recitation “said first interlayer insulation film has a first Young modulus and said second interlayer insulation film has a second, larger Young modulus than said first Young modulus” in claim 10. Such disclosure, however, does not remedy the deficiencies of Matsunaga discussed above.

For at least these reasons, claims 10-12 and 17-19 patentably distinguish over Matsunaga and APAF.

**Claim 20 was rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710) as applied to claim 1 above, and further in view of Pio (U.S. Patent No. 6,815,328).**

Claim 20 directly depends from claim 1.

Amendment under 37 CFR § 1.111  
Serial No. 10/780,701  
Attorney Docket No. 042113

Pio has been cited allegedly disclosing regarding claim 20 that an interconnect pillar structure is formed on a device isolation region. Such disclosure, however, does not remedy the deficiencies of Matsunaga discussed above regarding claim 1.

For at least these reasons, claim 20 patentably distinguishes over Matsunaga and Pio.

**Claim 21 was rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710) as applied to claim 1 above, and further in view of Sugiyama et al. (U.S. Patent Publication No. 2002/0040986 A1).**

Claim 21 directly depends from claim 1.

Sugiyama et al has been cited allegedly disclosing regarding claim 21 an interconnection layout in which the interconnect structure is formed diagonally in the multilayered structure of layers and within the boundaries of the pillar structure. Such disclosure, however, does not remedy the deficiencies of Matsunaga discussed above regarding claim 1.

For at least these reasons, claim 21 patentably distinguishes over Matsunaga and sugiyama et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

Amendment under 37 CFR § 1.111  
Serial No. 10/780,701  
Attorney Docket No. 042113

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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Enclosure: Replacement Sheets for Figs. 1-4

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